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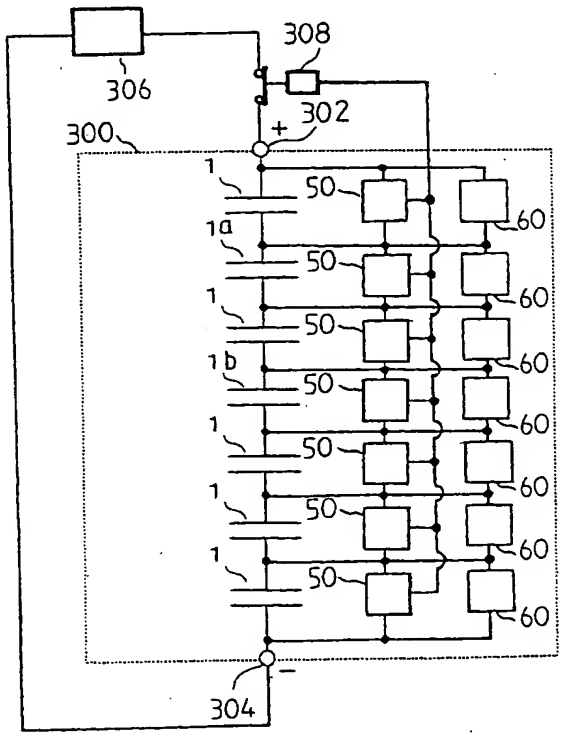
(54) Apparatus having plural electric double layer capacitors and method for adjusting voltages of the capacitors

(57) An electric double layer capacitor apparatus including a plurality of electric double layer capacitors connected in series, at least one set of a voltage detection device and a discharge device, and a controller. The at least one set is provided to at least one of the plurality of electric double layer capacitors. The voltage detection device is configured to detect a terminal voltage of the at least one of the plurality of electric double layer capacitors. The controller is configured to stop current for charging the plurality of electric double layer capacitors when the terminal voltage detected by the voltage detection device reaches a maximum charge voltage. The discharge device is configured to discharge the at least one of the plurality of electric double layer capacitors such that said terminal voltage drops toward a predetermined target voltage which is lower than the maximum charge voltage when the terminal voltage is higher than the predetermined target voltage, and the discharge device is configured not to discharge the at least one of the plurality of electric double layer capacitors when the terminal voltage is equal to or lower than the predetermined target voltage.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an electric double layer capacitor apparatus or system including a plurality of electric double layer capacitors and a method for adjusting voltages of the plurality of electric double layer capacitors.

Description of the Background

[0002] Power supplies which include a plurality of electric double layer capacitors are disclosed in U.S. Patent 5,783,928 (hereinafter referred to as the "'928 patent"), entitled "Storage Capacitor Power Supply"; U.S. Patent 5,982,050 (hereinafter referred to as the "'050 patent") , entitled "Power Supply Unit For Automotive Vehicle"; U.S. Patent 5,932,932 (hereinafter referred to as the "'932 patent"), entitled "Storage battery voltage control apparatus"; and Japanese Unexamined Patent Publication (Kokai) 10-201091 (hereinafter referred to as the "'091 publication"), entitled "Power Supply Unit For Automotive Vehicle Utilizing Electric Double Layer Capacitors." The contents of these applications are incorporated herein by reference in their entirety.

[0003] In an electric double layer capacitor apparatus disclosed in the '928 patent, referring to Fig. 13, an electric double layer capacitor apparatus includes a plurality of electric double layer capacitors 1 (hereinafter referred to as "a cell" or "cells"). Each cell 1 has a current bypass circuit 16 which is connected to each cell 1 in parallel. An operation voltage of the shunt regulator 7 is set at a maximum charge voltage (V_u) of the cell 1 by adjusting a ratio of resistance of the resistors (13 and 15). When the voltage between a positive and negative pole terminals (3A and 3B) of the cell 1 is equal to the maximum charge voltage (V_u), the shunt regulator 7 turns on and therefore current flows to the resistor 5. Accordingly, a PNP transistor 9 turns on and prevents all capacitors from being applied with voltages exceeding maximum charge voltage. When the voltage between the positive and negative pole terminals (3A and 3B) is equal to the maximum charge voltage (V_u).

[0004] In Fig. 13, it is supposed that capacitance (C1) of the cell (1a) is 1000 (F), capacitance (C2) of the cell (1b) is 1150 (F) and charge current is constant at 10 (A). Further, initial voltages of the cells (1a and 1b) are equal to zero (V) and the maximum charge voltage (V_u)is set at 2.5 (V) and equal to a uniform voltage.

[0005] Referring to Fig. 14, the voltage of the cell (1a) which has smaller capacitance becomes the maximum charge voltage (V_H) at (t1) before the voltage of the cell (1b) becomes the maximum charge voltage (V_H). Then, the voltage of the cell (1b) becomes the maximum charge voltage (V_H) at (t2) which is after (t1) by (Δt). (Δt) is approximately calculated as follows:

$$\Delta t = (C2\text{-}C1)^{*}V_H / I = 37.5 \text{ seconds.}$$

[0006] Heat of about 25 (W) generates in the bypass circuit (16) when bypass current flows for the period of Δt.

[0007] The '050 patent discloses a power supply unit which includes a plurality of electric double layer capacitors and a plurality of current bypass circuits which are connected to each cell in parallel, respectively. Each circuit has a Zener diode. The voltage of each cell is substantially adjusted to be Zener voltage.

[0008] The '091 reference discloses a power source which includes a plurality of electric double layer capacitors and a plurality of discharge circuits in order to adjust the voltage of each cell. Each discharge circuit is connected to each cell in parallel via a switch. When an accessary switch of a car is turned on, each switch connects each discharge circuit to each cell. Accordingly, the voltage of each cell is adjusted. Each switch may be manually turned on to discharge each cell after an engine stops.

[0009] The '932 reference discloses a storage battery voltage control apparatus which includes a plurality of electric double layer capacitors and a voltage-correcting storage battery over switches and a current-limiting resistor. In order to adjust the voltage of each cell, the voltages of each of the storage battery cells high in voltage can be equalized by transferring the charge to a storage battery cell low in voltage.

SUMMARY OF THE INVENTION

[0010] According to one aspect of the invention, an electric double layer capacitor apparatus or system includes a plurality of electric double layer capacitors connected in series, at least one set of a voltage detection device and a discharge device, and a controller. The at least one set is provided to at least one of the plurality of electric double layer capacitors. The voltage detection device is configured to detect a terminal voltage of the at least one of the plurality of electric double layer capacitors. The controller is configured to stop current for charging the plurality of electric double

layer capacitors when the terminal voltage detected by the voltage detection device reaches a maximum charge voltage. The discharge device is configured to discharge the at least one of the plurality of electric double layer capacitors such that said terminal voltage drops toward a predetermined target voltage which is lower than the maximum charge voltage when the terminal voltage is higher than the predetermined target voltage, and the discharge device is configured not to discharge the at least one of the plurality of electric double layer capacitors when the terminal voltage is equal to or lower than the predetermined target voltage.

[0011] According to another aspect of the invention, a method for adjusting voltages of a plurality of electric double layer capacitors, includes charging the plurality of electric double layer capacitors which are connected in series; detecting a terminal voltage of at least one of the plurality of electric double layer capacitors;

stopping charging the plurality of electric double layer capacitors when it is determined that the terminal voltage is equal to or higher than a maximum charge voltage; discharging the at least one of the plurality of electric double layer capacitors such that the terminal voltage drops toward a predetermined target voltage which is lower than the maximum charge voltage when the terminal voltage is higher than the predetermined target voltage; and preventing discharging the at least one of the plurality of electric double layer capacitors such that the terminal voltage is maintained when the terminal voltage is equal to or lower than the predetermined target voltage.

[0012] According to yet another aspect of the invention, a voltage control circuit for an electric double layer capacitor apparatus which comprises a plurality of electric double layer capacitors connected in series, includes at least one voltage detection circuit, a controlling circuit, at least one electric discharging circuit. The least one voltage detection circuit is configured to detect a terminal voltage of at least one of the plurality of electric double layer capacitors. The controlling circuit is configured to stop charging the plurality of electric double layer capacitors when it is determined that voltage of at least one of the plurality of electric double layer capacitors is equal to or higher than a maximum charge voltage based on the detected terminal voltage. The at least one electric discharging circuit is provided corresponding to the at least one voltage detection circuit. The at least one electric discharging circuit is configured to discharge electricity charged in adjustment capacitors among the plurality of electric double layer capacitors such that voltage of each of the adjustment capacitors drops toward a predetermined target voltage which is lower than the maximum charge voltage when said terminal voltage is higher than the predetermined target voltage.

[0013] According to a further aspect of the invention, a use of an electric double layer capacitors for a system includes a motor configured to operate the system, a plurality of electric double layer capacitors connected in series and configured to supply power to the motor, at least one set of a voltage detection device and a discharge device, and a controller. The at least one set is provided to at least one of the plurality of electric double layer capacitors. The voltage detection device is configured to detect a terminal voltage of the at least one of the plurality of electric double layer capacitors. The controller is configured to stop current for charging the plurality of electric double layer capacitors when the terminal voltage detected by the voltage detection device reaches a maximum charge voltage. The discharge device is configured to discharge the at least one of the plurality of electric double layer capacitors such that said terminal voltage drops toward a predetermined target voltage which is lower than the maximum charge voltage when the terminal voltage is higher than the predetermined target voltage, and the discharge device is configured not to discharge the at least one of the plurality of electric double layer capacitors when the terminal voltage is equal to or lower than the predetermined target voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] A more complete appreciation of the invention and many of the attendant advantages thereof will become readily apparent with reference to the following detailed description, particularly when considered in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 2 is a graph showing changes of voltages (V_a and V_b) of cells of the electric double layer capacitor apparatus shown in Fig. 1;

Fig. 3 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 4 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 5 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 6 is a graph showing changes of voltages of cells (1a and 1b) of the electric double layer capacitor apparatus shown in Fig. 5;

Fig. 7 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the

present invention;

Fig. 8 is a graph showing changes of voltages (V_a and V_b) of cells of the electric double layer capacitor apparatus shown in Fig. 7;

Fig. 9 is a flow chart for charging the cells of the electric double layer capacitor apparatus shown in Fig. 7;

Fig. 10 is a block diagram showing an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 11 is a flow chart for charging the cells of the electric double layer capacitor apparatus shown in Fig. 10;

Fig. 12 is a block diagram showing a vehicle having an electric double layer capacitor apparatus according to an embodiment of the present invention;

Fig. 13 is a block diagram showing a conventional electric double layer capacitor apparatus;

Fig. 14 is a graph showing changes of voltages of cells of the electric double layer capacitor apparatus shown in Fig. 13; and

Fig. 15 is a graph showing changes of voltages of cells of the electric double layer capacitor apparatus shown in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The preferred embodiments will now be described with reference to the accompanying drawings, wherein like reference numerals designate corresponding or identical elements throughout the various drawings.

[0016] Fig. 1 shows an electric double layer capacitor apparatus or system according to an embodiment of the present invention. Referring to Fig. 1, an electric double layer capacitor apparatus 300 includes a plurality of electric double layer capacitors 1 (hereinafter referred to as "a cell" or "cells"), and a plurality sets of voltage detection circuit 50 and discharge circuit 60. The electric double layer capacitor apparatus 300 further includes positive and negative terminals (302 and 304) which are connected to a power supply source 306 via a switch 308. The power supply source 306 is a current supply source, preferably constant current source to the electric double layer capacitor apparatus 300 in order to charge the cells 1. The power supply source 306 may supply current which is adjustable or changeable as time elapses. Also the power supply source 306 is preferably to be a constant current source. Each voltage detection circuit 50 is connected to positive and negative ends of each of all cells 1 and detects voltage of each cell 1. When voltage of any one of the cells 1 detected by a voltage detection circuit 50 is equal to or higher than a predetermined maximum charge voltage (V_u) of the cells 1, the voltage detection circuit 50 operates to open the switch 308. Accordingly, the power supply source 306 stops supplying electric power to the electric double layer capacitor apparatus 300.

[0017] Each discharge circuit 60 is connected to the positive and negative ends of each of all cells 1. When voltage of a cell 1 detected by a voltage detection circuit 50 is equal to or lower than an equalized voltage (V_e) which is lower than the maximum charge voltage (V_u), the discharge circuit 60 of that cell 1 is off and thus the cell 1 is not discharged through the discharge circuit 60. When voltage of a cell 1 detected by a voltage detection circuit 50 is higher than the equalized voltage (V_e), the discharge circuit 60 of that cell 1 turns on and thus the cell 1 is discharged through the discharge circuit 60 such that the voltage of the cell 1 becomes substantially equal to the equalized voltage (V_e). Accordingly, only cells 1 (voltage adjustment capacitors) whose voltages are higher than the equalized voltage (V_e) are discharged via the discharge circuits 60, respectively, to equalize voltages of the plurality of cells 1 at the equalized voltage (V_e). Accordingly, in this case, the equalized voltage (V_e) is a predetermined target voltage. When voltage of a cell 1 detected by a voltage detection circuit 50 is equal to or lower than the equalized voltage (V_e) during discharging, the discharge circuit 60 is off and thus the discharge of the cell 1 stops. Therefore, voltages of each cell 1 become equal to the equalized voltage (V_e).

[0018] In this embodiment, when voltage of a cell 1 is higher than the equalized voltage (V_e), the discharge circuit 60 of that cell 1 turns on and thus the cell 1 is discharged even though during the charging period. However, the discharge circuit 60 may be off during the charging period even though voltage of a cell 1 is higher than the equalized voltage (V_e) and may turn on after the charging period is complete and when voltage of a cell 1 is higher than the equalized voltage (V_e).

[0019] Further, the maximum charge voltage (V_u) and the equalized voltage (V_e) may be semi-fixed values or automatically changeable values according to environments or applications.

[0020] Fig. 2 illustrates changes of voltages (V_a and V_b) of cells 1, for example, cells (1a and 1b). All cells 1 are not necessarily charged to have voltages higher than the equalized voltage (V_e). Referring to Figs. 1 and 2, both cells (1a and 1b) are charged during a charge period (t_c) from (T_0) to (T_2). At (T_2), the voltage (V_a) of the cell (1a) becomes equal to the maximum charge voltage (V_u). Accordingly, at (T_2), the voltage detection circuit 50 operates to open the switch 308 and the power supply source 306 stops supplying current the electric double layer capacitor apparatus 300. When current stops, the voltage (V_a) of the cell (1a) drops by dropping voltage (V_{drop}), because the cell 1 has internal resistance (R_{in}) which is normally in the range of (mΩ). The dropping voltage (V_{drop}) is calculated as follows:

$V_{drop} = R_{in} * Ic$, where

Ic is charge current.

[0021] At (T_2), since the voltage (V_a) of the cell (1a) is higher than the equalized voltage (V_e), the discharge circuit 60 of the cell (1a) turns on and thus the cell (1a) is discharged through the discharge circuit 60. The cell (1a) is a discharge capacitor. The cell (1a) is discharged during a discharge period (t_D) from (T_2) to (T_3). On the other hand, from (T_2) to (T_3), since the voltage (V_b) of the cell (1b) is lower than the equalized voltage (V_e), the discharge circuit 60 of the cell (1b) is off and thus the cell (1b) is not discharged through the discharge circuit 60. At (T_3) during the discharge of the cell (1a), a load, for example, a motor connected to the electric double layer capacitor apparatus 300 is turned on. During a load period (t_L) from (T_3) to (T_5), the electric double layer capacitor apparatus 300 supplies power to the load. Both cells (1a and 1b) are again charged during a charge period (t_c) from (T_6) to (T_8). As this operation is repeated, voltages of all cells 1 are equalized at the equalized voltage (V_e) after being charged.

[0022] Fig. 15 is a more detailed graph of the graph shown in Fig. 2. Table 1 explains each timing in Fig. 15.

TIME	T_0	$T_0 - T_1$	T_1	$T_1 - T_2$	T_2
STATE	START CHARGING	Charging	Charging	Charging	STOP CHARGING
Disc-cir1	OFF	OFF	*ON*	*ON*	*ON*
Vc1	Vc1<Ve	V−UP	Vc1>Ve	V-UP	Vc1>Ve
Disc-cir2	OFF	OFF	OFF	OFF	OFF
Vc2	Vc2<Ve	V−UP	Vc2<Ve	V-UP	Vc2<Ve

$T_2 - T_3$	T_3	$T_3 - T_4$	T_4	$T_4 - T_5$	T_5
Waiting	START POWER Discharging	POWER Discharging	POWER Discharging	POWER Discharging	STOP POWER Discharging
ON	*ON*	*ON*	OFF	OFF	OFF
Adjustment	Vc1>Ve	V-down	Vc1>Ve	V-down	Vc1<Ve
OFF	OFF	OFF	OFF	OFF	OFF
HOLD	Vc2<Ve	V-down	Vc2<Ve	V-down	Vc2<Ve

$T_5 - T_6$	T_6	$T_6 - T_7$	T_7	$T_7 - T_8$	T_8
Waiting	START CHARGING	Charging	Charging	Charging	STOP CHARGING
OFF	OFF	OFF	*ON*	*ON*	*ON*
HOLD	Vc1<Ve	V-UP	Vc1>Ve	V-UP	Vc1>Ve
OFF	OFF	OFF	OFF	OFF	OFF
HOLD	Vc2<Ve	V-UP	Vc2<Ve	V-UP	Vc2<Ve

$T_8 - T_9$	T_9	$T_9 - T_{10}$	T_{10}	$T_{10} - T_{11}$	T_{12}
Waiting	START POWER Discharging	POWER Discharging	POWER Discharging	POWER Discharging	START CHARGING
ON	*ON*	*ON*	OFF	OFF	OFF
Adjustment	Vc1>Ve	V-down	Vc1<Ve	V-down	Vc1<Ve
OFF	OFF	OFF	OFF	OFF	OFF
HOLD	Vc2<Ve	HOLD	Vc2<Ve	V-down	Vc2<Ve

$T_{12} - T_{13}$	T_{13}	$T_{13} - T_{14}$	T_{14}	$T_{14} - T_{15}$	T_{15}
Charging	Charging	Charging	Charging	Charging	STOP CHARGING
OFF	*ON*	*ON*	*ON*	*ON*	*ON*
V-up	Vc1>Ve	V-up	Vc1>Ve	V-up	Vc1>Ve
OFF	OFF	OFF	*ON*	*ON*	*ON*
V-up	Vc2<Ve	V-up	Vc2>Ve	V-up	Vc2>Ve

$T_{15} - T_{16}$	T_{16}
Waiting	Waiting
ON	OFF
Adjustment	Vc1=Ve (equalized)
ON	OFF
Adjustment	Vc2=Ve (equalized)

[0023] The voltage detection circuit 50 and the discharge circuit 60 may be constructed as an analog circuit utilizing transistors and other discrete parts. In this case, circuits which have stable operations may be obtained at low costs. The voltage detection circuit may outputs voltage or current signals which represent the detected voltage. Also the volt-

age detection circuit 50 and the discharging circuit 60 may be constructed to be an IC.

[0024] Switching element of the discharge circuit is, for example, a transistor, another semiconductor or the like. When voltage of a cell 1 is higher than the equalized voltage (V_e), the switching element turns on to discharge the cell 1 via, for example, a resistor. On the other hand, when voltage of a cell 1 is equal to or lower than the equalized voltage (V_e), the switching element turns off and the cell 1 is not discharged.

[0025] The discharge circuit 60 does not necessarily operate while the cells 1 are charged. Accordingly, a resistor to which discharge current flows may have large resistance. Therefore, since a discharge current value may be small, an amount of heat generation of the resistor and power loss may be small. However, the discharge period during which the voltage of a cell 1 becomes equal to the equalized voltage (V_e) becomes longer as the resistance of the resistor increases. Accordingly, the resistance of the resistor is determined by balancing the discharge period and the heat amount. The resistor may be a variable resistor.

[0026] According to this embodiment of the present invention, because voltages of the cells 1 are equalized more precisely, the charging and power supplying ability of the electric double layer capacitor apparatus may be fully utilized and the apparatus may stably operates for a long period of time. Even though characteristics of the electric double layer capacitors are different, the electric double layer capacitor apparatus may be efficiently charged and discharged by compensating the characteristics differences.

[0027] Further, the maximum charge voltage and the predetermined target voltage may be determined for each cell according to characteristics of each cell.

[0028] Although each of all cells 1 has the voltage detection circuit 50 and the discharge circuit 60 as shown in Fig. 1, the electric double layer capacitor apparatus 300 may include only one voltage detection circuit 50 and one discharge circuit 60 as shown in Fig. 3. Referring to Fig. 3, one voltage detection circuit 50 and one discharge circuit 60 are connected to, for example, two cells 1 which are connected in series.

[0029] Further, as shown in Fig. 4, some of all cells 1 may have the voltage detection circuits 50 and one discharge circuits 60, respectively.

[0030] If the voltage detection circuits 50 and the discharge circuits 60 are disposed for only some portion among total cells, the portion is selected from the group of cells who have smaller capacitance than the other, relatively. For example, in total cells with certain dispersion of capacitance, one half of smaller capacitance are arranged to be connected to the voltage detection circuits 50 and the discharge circuits 60 and the other half having higher capacitance may be open without the voltage detection circuits 50 and the discharge circuit 60.

[0031] In case of two cells, the circuits are arranged for the cell having smaller capacitance. In this embodiment, the electric double layer capacitor apparatus 300 may include only one voltage detection circuit 50 which detects the terminal voltage of each of the plurality of the cells 1 by switching the connection between the one voltage detection circuit 50 and each of the plurality of the cells 1.

[0032] Fig. 5 shows an electric double layer capacitor apparatus according to an embodiment of the present invention. Referring to Fig. 5, an electric double layer capacitor apparatus 300 includes a plurality of electric double layer capacitors 1. Since the plurality of cells 1 include same constructions, a circuit will be explained hereinafter with respect to a cell (1a).

[0033] A terminal (27b) of a first shunt regulator 27 is connected to a positive pole terminal (3A) of the cell (1a). Another terminal (27a) of the first shunt regulator 27 is connected to a negative pole terminal (3B) of the cell (1a) via a resistor 25. Further, the terminal (27a) of the first shunt regulator 27 is connected to a base of a first NPN transistor 29. A terminal (27c) of the first shunt regulator 27 is connected to one end of a resistor 21 and one end of a resistor 23. Another end of the resistor 21 is connected to the positive pole terminal (3A) of the cell (1a). Another end of the resistor 23 is connected to the negative pole terminal (3B) of the cell (1a).

[0034] An emitter of the first transistor 29 is connected to the negative pole terminal (3B) of the cell (1a). A collector of the first transistor 29 is connected to the positive pole terminal (3A) of the cell (1a) via a photocoupler 31.

[0035] A terminal (37b) of a second shunt regulator 37 is connected to the positive pole terminal (3A) of the cell (1a). Another terminal (37a) of the second shunt regulator 37 is connected to the negative pole terminal (3B) of the cell (1a) via a resistor 35. Further, the terminal (37a) of the second shunt regulator 37 is connected to a base of a second NPN transistor 39. A terminal (37c) of the second shunt regulator 37 is connected to one end of a resistor 41 and one end of a resistor 43. Another end of the resistor 41 is connected to the positive pole terminal (3A) of the cell (1a) . Another end of the resistor 43 is connected to the negative pole terminal (3B) of the cell (1a).

[0036] A collector of the second transistor 39 is connected to the positive pole terminal (3A) of the cell (1a). An emitter of the second transistor 39 is connected to the negative pole terminal (3B) of the cell (1a) via a resistor 45.

[0037] All of the cells 1 and all of the circuits are contained in a box to constitute an electric double layer capacitor apparatus 300. The electric double layer capacitor apparatus 300 further includes positive and negative terminals (302 and 304) which are connected to a power supply source 306 via a switch 308. The switch 308 is controlled by the photocoupler 31. The power supply source 306 is configured to supply current to the electric double layer capacitor apparatus 300 in order to charge the cells 1.

[0038] An operation voltage of the first shunt regulator 27 is set at the maximum charge voltage (V_u) of the cell 1. The operation voltage may be determined by adjusting a ratio of resistance of the resistors (21 and 23). When the voltage between the positive and negative pole terminals (3A and 3B) is equal to or higher than the maximum charge voltage (V_u), the first shunt regulator 27 turns on and therefore current flows to the resistor 25. The first transistor 29 amplifies a signal which shows that the voltage between the positive and negative pole terminals (3A and 3B) is equal to or higher than the maximum charge voltage (V_u). According to the signal, the photocoupler 31 operates to open the switch 308. Accordingly, the power supply source 306 stops to supply electric power to the electric double layer capacitor apparatus 300.

[0039] An operation voltage of the second shunt regulator 37 is set at the equalized voltage (V_e) which is lower than the maximum charge voltage (V_u). The equalized voltage (V_e) is determined based on a ratio of resistance of the resistors (41 and 43). When the voltage between the positive and negative pole terminals (3A and 3B) of a cell 1 is higher than the equalized voltage (V_e) after the power supply source 306 stops the power supply to the electric double layer capacitor apparatus 300, the second shunt regulator 37 turns on and therefore current flows to the resistor 35. Accordingly, the second transistor 39 turns on and thus the cell 1 discharges through the resistor 45. When the voltage between the positive and negative pole terminals (3A and 3B) of the cell 1 is equal to or lower than the equalized voltage (V_e), the second shunt regulator 37 turns off and therefore the second transistor 39 turns off. Accordingly, the cell 1 maintains its voltage at that voltage.

[0040] The second transistor 39 turns on even during the charging period of the cell 1 when the voltage between the positive and negative pole terminals (3A and 3B) is higher than the equalized voltage (V_e). However, the resistor 45 may have large resistance because the resistor 45 does not have a function of bypassing the cell 1 while cells 1 are charged. Accordingly, since the resistor 45 has large resistance, a power consumption of the resistor 45 is small. Therefore, there is no problem even though the second transistor 39 turns on during the charging period of the electric double layer capacitor 1.

[0041] The circuit may be constructed such that the second transistor 39 does not turn on during the charging period of the cell 1 and turns on when the charging period is complete and when the voltage between the positive and negative pole terminals (3A and 3B) is higher than the equalized voltage (V_e).

[0042] According to this embodiment of the present invention, because voltages of the cells 1 are equalized more precisely, the charging and power supplying ability of the electric double layer capacitor apparatus may be fully utilized and the apparatus may stably operates for a long period of time. Even though characteristics of the electric double layer capacitors are different, the electric double layer capacitor apparatus may be efficiently charged and discharged by compensating the characteristics differences.

[0043] Although shunt regulators are utilized in this embodiment, other semiconductors which has similar reference voltage accuracy may be utilized.

[0044] Fig. 7 shows an electric double layer capacitor apparatus according to an embodiment of the present invention. Referring to Fig. 7, an electric double layer capacitor apparatus 300 includes a plurality of electric double layer capacitors 1, discharge circuits 60 corresponding to respective cells 1, a voltage detection circuit 50, an electronic control unit 70, a current detection circuit 80, and a switching circuit 90. The electric double layer capacitor apparatus 300 further includes positive and negative terminals (302 and 304) which are connected to a power supply source 306. The power supply source 306 is configured to supply current to the electric double layer capacitor apparatus 300 in order to charge the cells 1.

[0045] The electronic control unit 70 is constructed as a microprocessor and includes a ROM (read only memory) 72, a RAM (random access memory) 73, a CPU (micro-processor) 74, an input port 75, and an output port 76. The ROM 72, the RAM 73, the CPU 74, the input port 75, and the output port 76 are interconnected via a bidirectional bus 71.

[0046] The discharge circuit 60 is configured to discharge the corresponding cell 1 and connected to the output port 76. The voltage detection circuit 50 is configured detect voltage of each cell 1 and connected to the input port 75. The current detection circuit 80 is configured detect the current of the electric double layer capacitor apparatus 300 and connected to the input port 75. The switching circuit 90 is configured to stop the power supply to the electric double layer capacitor apparatus 300 from the power supply source 306 and connected to the output port 76.

[0047] Fig. 8 illustrates changes of voltages (V_a and V_b) of cells 1, for example, cells (1a and 1b). Referring to Figs. 7 and 8, during a load period (t_L) from (T_{20}) to (T_{21}), the electric double layer capacitor apparatus 300 supplies power to the load. Accordingly, voltages of both cells (1a and 1b) decrease. Before charging the cells 1, voltage differences (ΔV_a and ΔV_b) are calculated such that the voltages (V_a and V_b) of both cells (1a and 1b) become equal to the maximum charge voltage (V_u) substantially simultaneously while being charged. During a discharge period (t_D) from (T_{22}) to (T_{23}), both cells (1a and 1b) are discharged such that each voltage (V_a or V_b) reduce by the voltage difference (ΔV_a or ΔV_b). During a charge period (t_C) from (T_{23}) to (T_{24}), both cells (1a and 1b) are charged. The voltages (V_a and V_b) of both cells (1a and 1b) become equal to the maximum charge voltage (V_u) at (T_{24}) at the same time. In this case, the maximum charge voltage (V_u) is equal to the equalized voltage (V_e).

[0048] Fig. 9 is a flow chart for charging the cells 1. Referring to Figs. 7 and 9, at step (S1), capacitance (Ci) of each cell 1 is calculated based on a change (ΔQ) of charge amount and a change (ΔV) of voltage according to the following equation.

$$Ci = \Delta Q / \Delta V$$

[0049] The changes (ΔQ) of charge amounts are calculated based on current detected by the current detection circuit 80. The changes (ΔV) of voltage are calculated based on the voltage detected by the voltage detection circuit 50.

[0050] At step (S2), a charge amount (Qi) for each cell 1 which is necessary to increase the voltage of each cell 1 to the maximum charge voltage (V_u) is calculated according to the following equation:

$$Qi = Ci * (V_u - Vi)$$

where Vi is voltage of each cell 1 at that time.

[0051] At step (S3), the maximum charge amount (Qmax) among the charge amounts (Qi) is determined. At step (S4), each charge amount difference (ΔQi) between the maximum charge amount (Qmax) and each charge amount (Qi) is calculated.

[0052] At step (S5), each voltage difference (ΔVi) is calculated according to the following equation.

$$\Delta Vi = \Delta Qi / Ci$$

[0053] At step (S6), the electronic control unit 70 controls each discharge circuit 60 to discharge each cell 1 such that the voltage (Vi) of each cell is decreased by each voltage difference (ΔVi). Then, at step (S7), the electronic control unit 70 turns on the switching circuit 90. Accordingly, the power supply source 306 supplies substantial constant current to the electric double layer capacitor apparatus 300 in order to charge the cells 1.

[0054] At step (S8), the electronic control unit 70 determines whether charging amount (Q) during this charge period is equal to or higher than the maximum charge amount (Qmax). When the charging amount (Q) is smaller than the maximum charge amount (Qmax), the power supply source 306 continues to supply constant current to the electric double layer capacitor apparatus 300. When the charging amount (Q) is equal to or higher than the maximum charge amount (Qmax), the routine goes to step (S9). At step (S9), the electronic control unit 70 turns off the switching circuit 90. Accordingly, the power supply source 306 stops supplying constant current to the electric double layer capacitor apparatus 300.

[0055] According to this embodiment of the present invention, because voltages of the cells 1 are equalized at the maximum charge voltage (V_u), the charging and power supplying ability of the electric double layer capacitor apparatus may be fully utilized.

[0056] In Step 9 (S9) the stop operation of supplying current to the electric double layer capacitor apparatus 300 may be done when the voltage of cell 1 is detected to be equal to the maximum charge voltage (V_u) by the voltage detection circuit 50. After stopping the charging current, the terminal voltage of cell 1 drops about I*R voltage drop (I_c*R_{in}) from the maximum charge voltage (V_u).

[0057] Fig. 10 shows an electric double layer capacitor apparatus according to an embodiment of the present invention. Referring to Fig. 10, an electric double layer capacitor apparatus 300 includes a plurality of electric double layer capacitors 1, discharge circuits 60 corresponding to respective cells 1, a voltage detection circuit 50, an electronic control unit 70, and a bypass circuit 100. The electric double layer capacitor apparatus 300 further includes positive and negative terminals (302 and 304) which are connected to a power supply source 306. The power supply source 306 is configured to supply constant current to the electric double layer capacitor apparatus 300 in order to charge the cells 1.

[0058] The bypass circuit 100 is connected to the cells 1 in parallel and configured to bypass all cells 1.

[0059] Fig. 11 is a flow chart for charging the cells 1. Basically, the operation of this embodiment is similar to the embodiment shown in Figs. 7-9. Referring to Figs. 10 and 11, at step (S20), capacitance (Ci) of each cell 1 is read from the ROM 72. The capacitance (Qi) of each cell 1 have been memorized in the ROM 72.

[0060] At step (S21), a charge time (T_C) during which the maximum charge amount (Qmax) is charged to a cell 1 is calculated. Then, at step (S22), the electronic control unit 70 opens the bypass circuit 100. Accordingly, the power supply source 306 supplies constant current to the cells 1 in order to charge the cells 1.

[0061] At step (S23), the electronic control unit 70 determines whether the charge time (T_C) has elapsed since the charge of the cells 1 started. When the electronic control unit 70 determines that the charge time (T_C) has not elapsed, the power supply source 306 continues to supply substantial constant current to the cells 1. When the electronic control unit 70 determines that the charge time (T_C) has elapsed, the routine goes to step (S24). At step (S24), the electronic control unit 70 closes the bypass circuit 100. Accordingly, the power supply source 306 stops supplying constant current to the cells. At this time, voltages of all cells become equal to the maximum charge voltage (V_u) at the same time.

[0062] In step (S24) the stop operation of supplying current to the electric double layer capacitor apparatus 300 may be done when the voltage of cell 1 is detected to be equal to the maximum charge voltage (V_u) by the voltage detection circuit 50. After stopping the charging current, the terminal voltage of cell 1 drops about I*R voltage drop (I_c*R_{in}) from the maximum charge voltage (V_u).

[0063] In the above embodiments, it is preferable to provide a voltage detection circuit 50 and a discharge circuit 60 to each of all cells 1 in order to control voltage of the cells more accurately.

[0064] The number of the cells 1 is determined considering the maximum charge voltage of the electric double layer capacitor apparatus 300. The endurance voltage of a cell 1 whose electrolytic solution is organic solution is about 3 (V). The endurance voltage of a cell 1 whose electrolytic solution is water solution is about 1 (V). Capacitance values of several (F) to tens of thousands (F) are available. For example, when the maximum charge voltage is from DC 750 (V) to 5,000 (V), it is preferable to determine the number of cells 1 to be from 188 to 3025. When the maximum charge voltage is from AC 100 (V) to 600 (V), it is preferable to determine the number of cells 1 to be from 36 to 512. For a general low voltage power source for controlling, it is preferable to determine the number of cells 1 to be from 3 to 30.

[0065] It is preferable to determine that the voltage range in which voltage of a cell 1 is adjustable by discharging the cell 1 via a discharge circuit 60 is from 50 (mV) to 900 (mV). The voltage range is determined considering both a frequency of the voltage equalization discharge and power loss because of the discharge.

[0066] It is preferable that relative dispersion of capacitance of cells 1 is within ±20%. It is more preferable that the relative dispersion of capacitance of cells 1 is within ±15%. If the relative dispersion is too large, the time to equalize voltages of cells 1 increases and thus power loss increases.

[0067] Furthermore, it is preferable that charge current is larger than 10 (A). It is more preferable that charge current is larger than 25 (A), because superior characteristics of an electric double layer capacitor may be utilized.

[0068] The electric double layer capacitor apparatus according to the present invention may be suitably utilized as a power source for systems. It is preferable that such systems are not operated during nighttime, such as, for example, elevators. During daytime, charging the electric double layer capacitor apparatus and supplying power from the electric double layer capacitor apparatus to a load are repeated. During this period, the discharge circuit consume a little power. During a long period in which the load is not operated, for example, during nighttime, voltages of the cells are slowly equalized. Therefore, dispersion of the voltages of the cells are compensated.

[0069] The electric double layer capacitor apparatus according to the present invention may be further utilized as a power source for systems which have motors, for example, electric cars, hybrid cars, electric trains and the like.

[0070] Fig. 12 shows an electric car 400. The car 400 includes a motor 410 and inverter 430, generator or battery 440 for rotating wheels 420, and an electric double layer capacitor apparatus 300 which supplies power to the motor 410 and reserves the output power of regenerative breaking.

[0071] According to the embodiments of the present invention, because voltages of the cells 1 are equalized more precisely, the charging and power supplying ability of the electric double layer capacitor apparatus may be fully utilized.

Example 1

[0072] In the embodiment as shown in Fig. 5, it is supposed that the number of cells 1 is two, the capacitance (C_1) of first cell (1a) is 1000 (F), the capacitance (C_2) of second cell (1b) is 1150 (F), the maximum charge voltage (V_u) is 2.5 (V), the charge current is constant current of 10 (A), the equalization voltage (V_e) is 2.1 (V), the initial voltage of the first and second cells (1a and 1b) is 0 (V), and the resistance (R) of the resistor 45 is 100 (Ω). The cell is a type of organic electrolytic solution.

[0073] Referring to Figs. 5 and 6, the voltages of the first and second cells (1a and 1b) linearly increase because the charge current is constant. At (t_2), the voltage (V_a) of the first cell (1a) which has smaller capacitance becomes equal to the maximum charge voltage (V_u) of 2.5 (V) first. Accordingly, at (t_2), the first transistor 29 turns on and thus the photocoupler 31 operates to open the switch 308. Accordingly, the power supply source 306 stops to supply electric power to the electric double layer capacitor apparatus 300. At this time, the voltage of the second cell (1b) is 2.17 (V).

[0074] When the voltages of the first and second cells (1a and 1b) are higher than the equalized voltage (V_e) of 2.1 (V), the second NPN transistor 39 turns on. (t_0) is about 210 seconds and (t_1) is about 242 seconds. The second cell (1b) is discharged until (t_3) at which the voltage of the second cell (1b) becomes equal to 2.1 (V). Similarly, the first cell (1a) is discharged until (t_4).

[0075] The voltages (V_{c1} and V_{c2}) of the first and second cells (1a and 1b) between (t_2) and (t_4) or (t_3) is calculated as follows:

$$V_{c1} \approx 2.5 \exp(-t/\tau_1),$$

$$\tau_1 \approx R * C_1 = 100\ (\Omega) * 1000\ (F) = 10^5 \text{ seconds},$$

$V_{c2} \approx 2.17 \exp(-t/\tau_2)$, and

$\tau_2 \approx R * C_2 = 100\ (\Omega) * 1150\ (F) = 1.15 \times 10^5$ seconds, where (t) is a period of time from (t_2).

[0076] Accordingly, (t_3) is about 4000 seconds and (t_4) is about 18000 seconds. The maximum discharge current (i_1) of the first cell (1a) is about 25 (mA) ($i_1 \approx 2.5$ (V) / 100 (Ω) = 25 (mA)). The maximum discharge current (i_2) of the second cell (1b) is about 22 (mA) ($i_2 \approx 2.17$ (V) / 100 (Ω) = 22 (mA)).

[0077] Because the discharge current is small, the power consumption and heat generation of the discharge circuit 60 which includes the NPN transistor 39 and the resistor 45 is small. The maximum power consumption (P) is 2.5 (V) * 25 (mA) = 62.5 (mW).

[0078] Further, the discharge circuit 60 discharges, for example, the first cell (1a) between (t_0) and (t_2). However, because the discharge current (25 (mA)) is considerably small comparing to the charge current (10 (A)), the discharge during the charging period may be neglected.

[0079] As described above, even though capacitances of the cells 1 are different, voltages of the cells 1 are maintained at the equalized voltage (V_e) after the cells 1 are discharged. Namely, voltages of the cells 1 are equalized at the equalized voltage (V_e).

[0080] In Fig. 6, the voltages (V_{c1} and V_{c2}) of the first and second cells (1a and 1b) are higher than the equalized voltage (V_e) when charging is complete. However, all of the cells 1 necessarily are charged to have voltages higher than the equalized voltage (V_e). Namely, cells 1 (discharge capacitors) whose voltages are higher than the equalized voltage (V_e) are discharged such that the voltages are equal to the equalized voltage (V_e). On the other hand, cells 1 whose voltages are lower than the equalized voltage (V_e) are not discharged and maintained at those voltages. Accordingly, as the this operation repeats, voltages of all cells are equal to the equalized voltage (V_e).

Example 2

[0081] In the embodiment as shown in Fig. 5, referring to Tables 2 and 3, it is supposed that the number of cells 1 is three, the capacitance (C_1) of a first cell is 1225 (F), the capacitance (C_2) of a second cell is 1204 (F), the capacitance (C_3) of a third cell is 1185 (F), an internal resistance of the first cell is 2.3(mΩ), an internal resistance of the second cell is 2.1(mΩ), an internal resistance of the third cell is 2.2(mΩ), the maximum charge voltage (V_u) is 2.5 (V), the charge current is constant current of 25 (A), the equalization voltage (V_e) is 2.4 (V), and the discharge resistance (R) of the resistor 45 is 5(Ω). In this example 2, the equalization of the three terminal voltage is achieved within 20 mV in one state and within 10 mV in another state.

Table 2

Cell	Capacitance [F]	Internal Resistance [mΩ]	Vv [V]	Ve [V]
C_1	1225	2.3	2.50	2.40
C_2	1204	2.1	2.50	2.40
C_3	1185	2.2	2.50	2.40

Table 3

	1	2	3	4	5	6	7	8
	Initial	After Charge	Before Equalizaion	After Equal-ization	After Dis-charge Power	After Charge	Before Equaliza-tion	After Equal-ization
Time	Approx. 1.5 min.		Approx. 2.5 min.		Approx. 1 min.	Approx. 1 min.	Approx. 2.5 min.	
C_1	0.28	2.42	2.38	2.38	1.03	2.45	2.42	2.40
C_2	0.34	2.47	2.41	2.40	1.01	2.50	2.46	2.40

Table 3 (continued)

	1	2	3	4	5	6	7	8
	Initial	After Charge	Before Equalizaion	After Equal-ization	After Dis-charge Power	After Charge	Before Equaliza-tion	After Equal-ization
Time	Approx. 1.5 min.		Approx. 2.5 min.		Approx. 1 min.	Approx. 1 min.	Approx. 2.5 min.	
C_3	0.24	2.50	2.46	2.40	0.99	2.47	2.45	2.40
Note: Resistance of Discharge Resistor: $RC_1=RC_2=RC_3=5\Omega$ Charge Current Ic=25A, Discharge Current Id=25A								

Example 3

[0082] In an example of Table 4, the resistance of the discharge resistor for the third cell is 1(Ω). In this example 3, the equalization of the three terminal voltages is achieved within 10 mV in one state.

Table 4

	1	2	3	4
	Initial	After Charge	Before Equalization	After Equalization
Time	Approx. 2 min.		Approx. 1 min.	
C_1	0.18	2.43	2.40	2.40
C_2	0.22	2.47	2.42	2.40
C_3	0.20	2.50	2.48	2.40
Note: Resistance of Discharge Resistor: $RC_1=RC_2=5\Omega$ $RC_3=1\Omega$ Charge Current Ic=25A				

[0083] Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

Claims

1. An electric double layer capacitor apparatus (300) comprising:

a plurality of electric double layer capacitors (1; 1a; 1b) connected in series;
at least one set of voltage detection device (50) and a discharge device (60), the at least one set being provided to at least one of the plurality of electric double layer capacitors (1; 1a; 1b), the voltage detection device (50) being configured to detect a terminal voltage of said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) ;
a controller (50; 70) configured to stop charging the plurality of electric double layer capacitors (1; 1a; 1b) when said terminal voltage detected by the voltage detection device (50) reaches a maximum charge voltage (V_u) ; and
the discharge device (60) being configured to discharge said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) such that said terminal voltage drops toward a predetermined target voltage (V_e) which is lower than the maximum charge voltage (V_u) when said terminal voltage is higher than the predetermined target voltage (V_e), and the discharge device (60) being configured not to discharge said at least one of the plu-

rality of electric double layer capacitors (1, 1a; 1b) when said terminal voltage is equal to or lower than the predetermined target voltage (V_e).

2. An electric double layer capacitor apparatus according to Claim 1, wherein terminal voltages of the plurality of electric double layer capacitors (1; 1a; 1b) are to be substantially equalized to said predetermined target voltage (V_e) in a state.

3. An electric double layer capacitor apparatus according to Claim 1, wherein the maximum charge voltage (V_u) is set to be an equalized voltage to which terminal voltages of the plurality of electric double layer capacitors (1; 1a; 1b) is to be substantially equalized in a state.

4. An electric double layer capacitor apparatus according to any Claim for Claims 1 through 3, wherein the at least one set of the voltage detection device 50 and the electric discharge device 60 is provided to each of all of the plurality of electric double layer capacitors (1; 1a; 1b).

5. An electric double layer capacitor apparatus according to any Claims of Claim 1 through 4, wherein the plurality of electric double layer capacitors (1; 1a; 1b) are charged by supplying substantially constant current.

6. An electric double layer capacitor apparatus according to any Claim of Claims 1 through 5, wherein the discharge device comprises a resistor whose resistance is 1 to 100 (Ω) and through which said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) is discharged.

7. An electric double layer capacitor apparatus according to any Claim of Claim 1 through 6, wherein the voltage detection device (50) comprises,

a first detection portion which is configured to detect the maximum charge voltage (V_u), and
a second detection portion which is configured to detect the predetermined target voltage (V_e).

8. An electric double layer capacitor apparatus according to any Claim of Claim 1 through 7, wherein a number of the plurality of electric double layer capacitors (1; 1a; 1b) is from 36 to 3025, and wherein discharge initial voltage of the electric double layer capacitor apparatus is at least 100 (V).

9. An electric double layer capacitor apparatus according to any Claim of Claims 1 through 7, wherein a number of the plurality of electric double layer capacitors is from 3 to 30, and wherein discharge initial voltage of the electric double layer capacitor apparatus is at most 50 (V).

10. An electric double layer capacitor apparatus according to any Claim of Claims 1 through 9, wherein relative dispersion of capacitances of the plurality of electric double layer capacitors is within ±20%.

11. A method for adjusting voltages of a plurality of electric double layer capacitors (1; 1a; 1b), comprising:

charging the plurality of electric double layer capacitors (1; 1a; 1b) which are connected in series;
detecting a terminal voltage of at least one of the plurality of electric double layer capacitors (1; 1a; 1b);
stopping charging the plurality of electric double layer capacitors (1; 1a; 1b) when it is determined that said terminal voltage is equal to or higher than a maximum charge voltage (V_u);
discharging said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) such that said terminal voltage drops toward a predetermined target voltage (V_e) which is lower than the maximum charge voltage (V_u) when said terminal voltage is higher than the predetermined target voltage (V_e) ; and
preventing discharging said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) such that said terminal voltage is maintained when said terminal voltage is equal to or lower than the predetermined target voltage (V_e).

12. A voltage control circuit for an electric double layer capacitor apparatus (300) which comprises a plurality of electric double layer capacitors (1, 1a; 1b) connected in series;
comprising;

at least one voltage detection circuit (50) configured to detect a terminal voltage of at least one of the plurality of electric double layer capacitors (1, 1a; 1b);

a controlling circuit (50; 70) configured to stop charging the plurality of electric double layer capacitors (1, 1a; 1b) when it is determined that voltage of at least one of the plurality of electric double layer capacitors (1; 1a, 1b) is equal to or higher than a maximum charge voltage (V_u) based on the detected terminal voltage; and

at least one electric discharging circuit (60) provided corresponding to the at least one voltage detection circuit (50) and for discharging electricity charged in adjustment capacitors among the plurality of electric double layer capacitors (1; 1a; 1b) such that voltage of each of the adjustment capacitors drops toward a predetermined target voltage (V_e) which is lower than the maximum charge voltage (V_u) when said terminal voltage is higher than the predetermined target voltage (V_e).

13. A Use of an electric double layer capacitor apparatus (300) for a system comprising:

a motor configured to operate the system;
a plurality of electric double layer capacitors (1; 1a; 1b) connected in series and configured to supply power to the motor;
at least one set of a voltage detection device (50) and a discharge device (60), the at least one set being provided to at least one of the plurality of electric double layer capacitors (1; 1a; 1b), the voltage detection device (50) being configured to detect a terminal voltage of said at least one of the plurality of electric double layer capacitors (1; 1a; 1b);
a controller (50; 70) configured to stop charging the plurality of electric double layer capacitors (1; 1a, 1b) when said terminal voltage detected by the voltage detection device (50) reaches a maximum charge voltage (V_u) ; and
the discharge device being (60) configured to discharge said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) such that said terminal voltage drops toward a predetermined target voltage (V_e) which is lower than the maximum charge voltage (V_u) when said terminal voltage is higher than the predetermined target voltage (V_e), and the discharge device (60) being configured not to discharge said at least one of the plurality of electric double layer capacitors (1; 1a; 1b) when said terminal voltage is equal to or lower than the predetermined target voltage (V_e).

FIG. 1

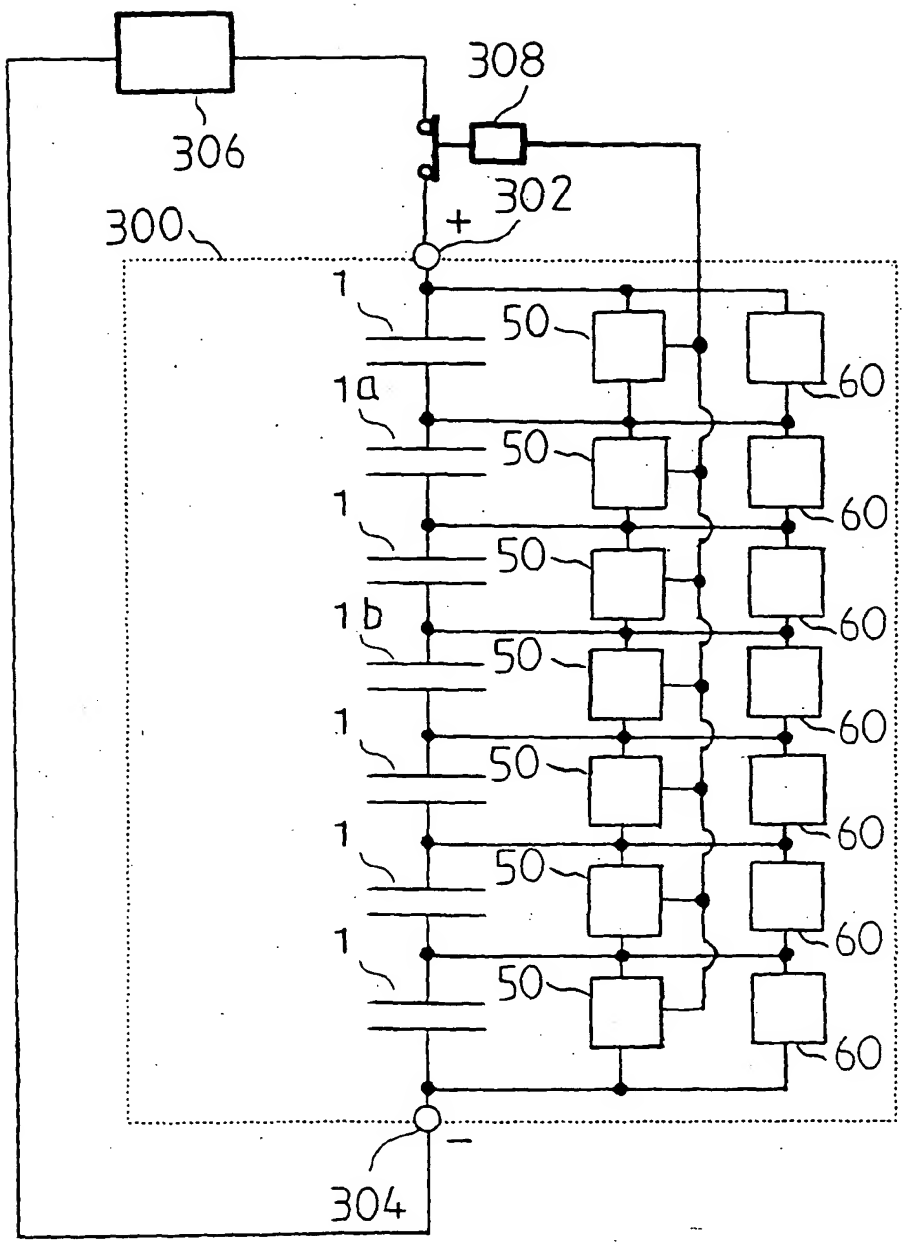


FIG. 2

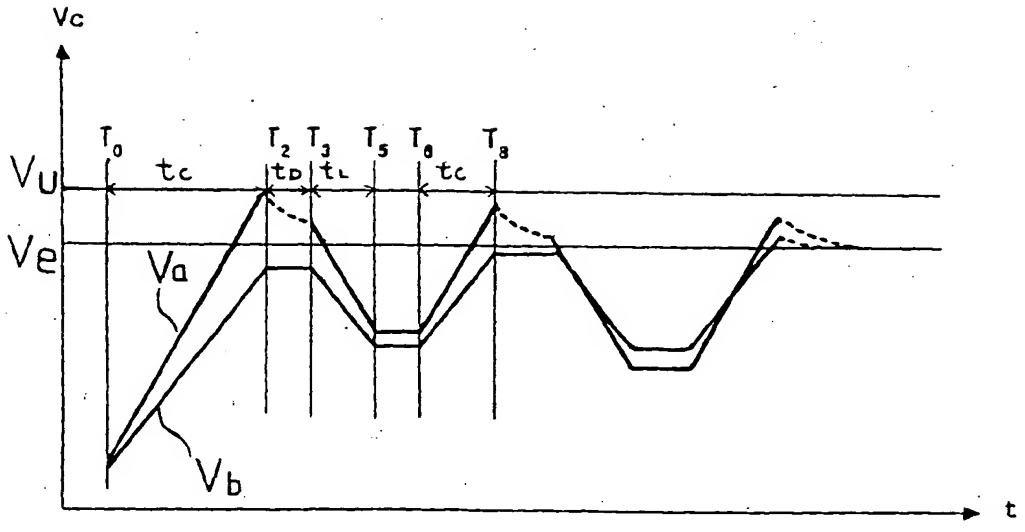


FIG. 3

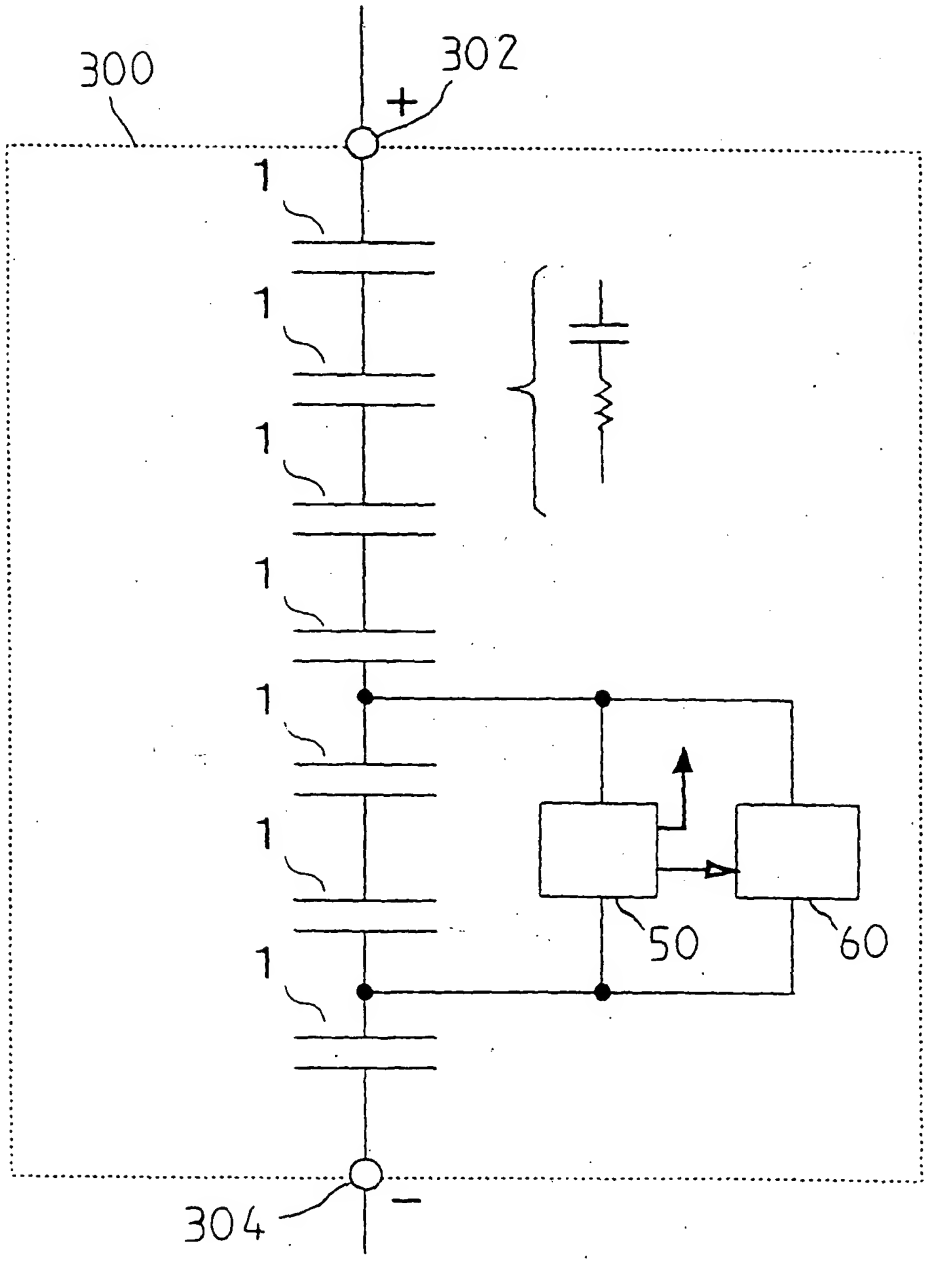


FIG. 4

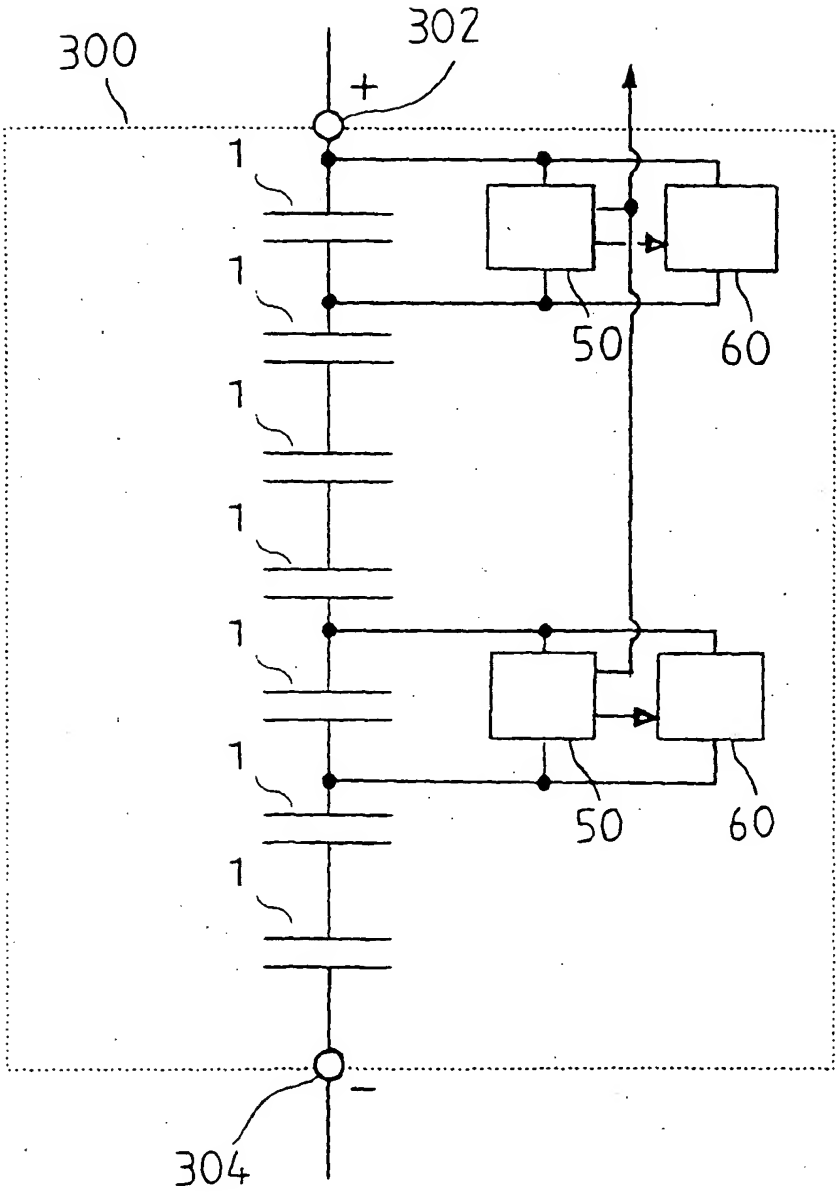


FIG. 5

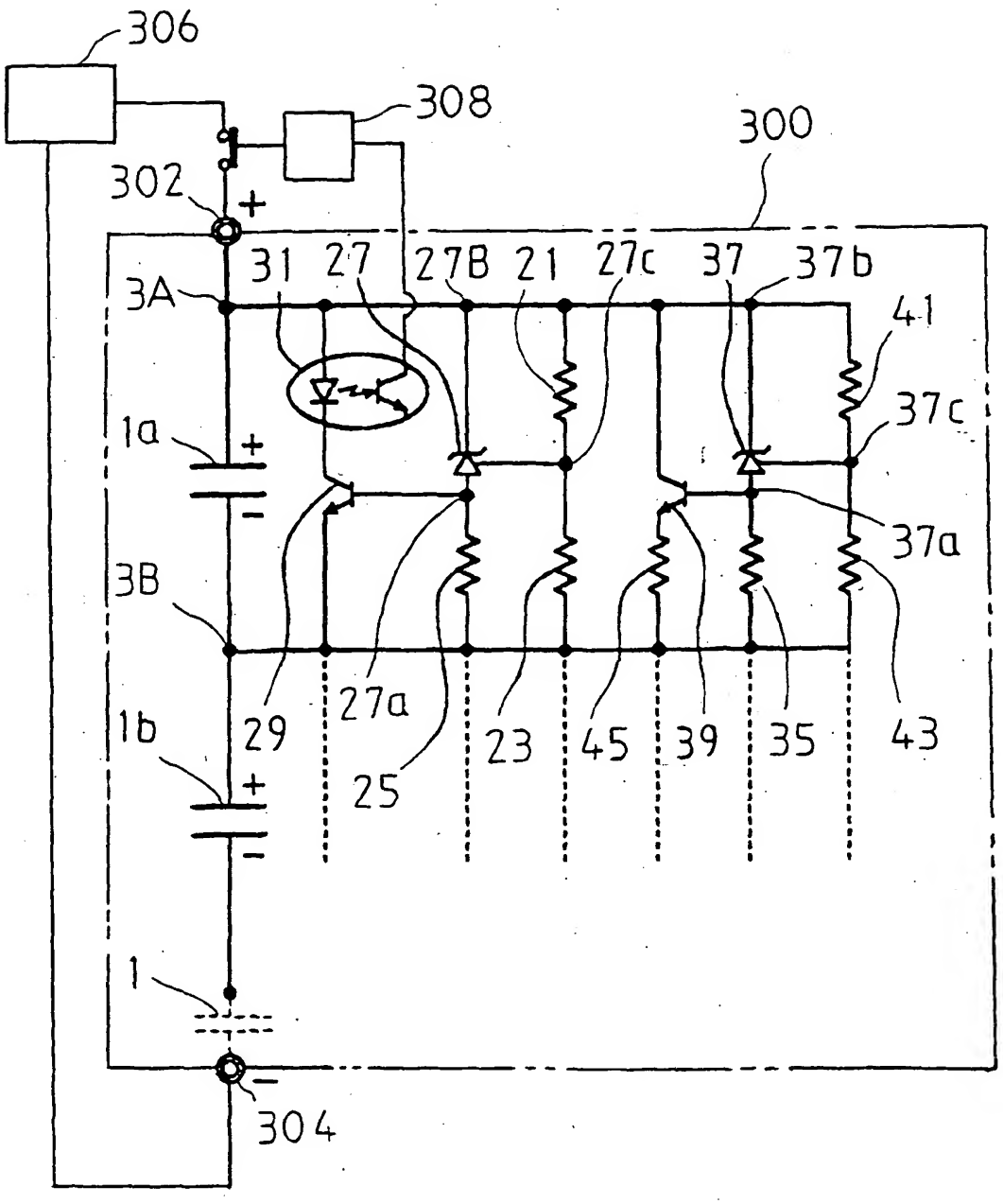

306
308
300
302
+
31
27
27B
21
27c
37
37b
3A
41
37c
1a
+
−
37a
3B
29
27a
25
23
45
39
35
43
1b
+
−
1
−
304

FIG. 6

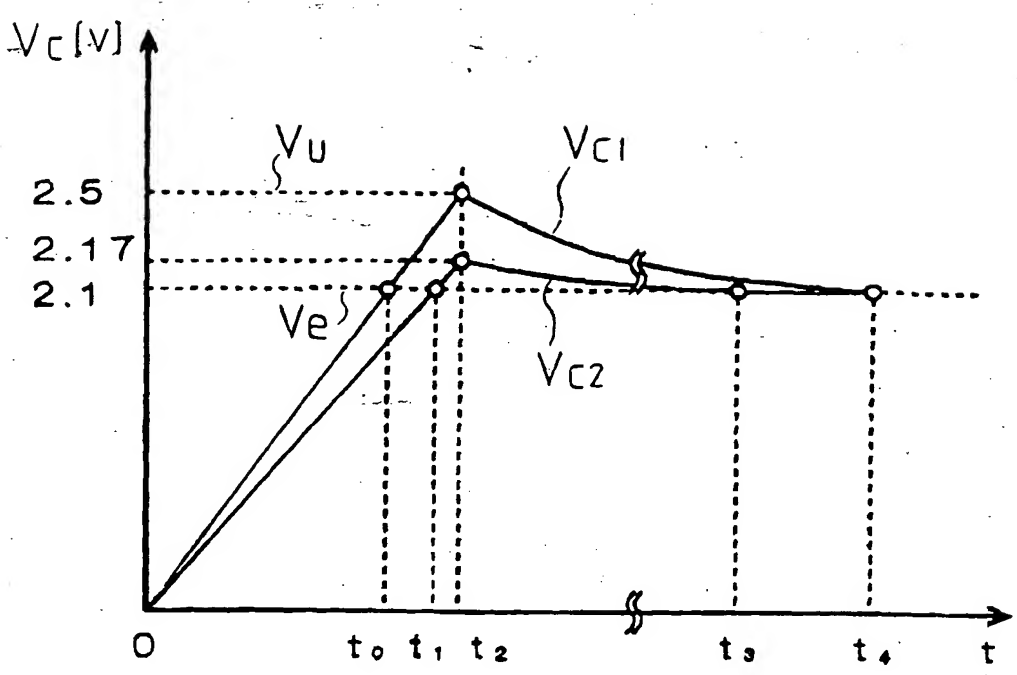


FIG. 7

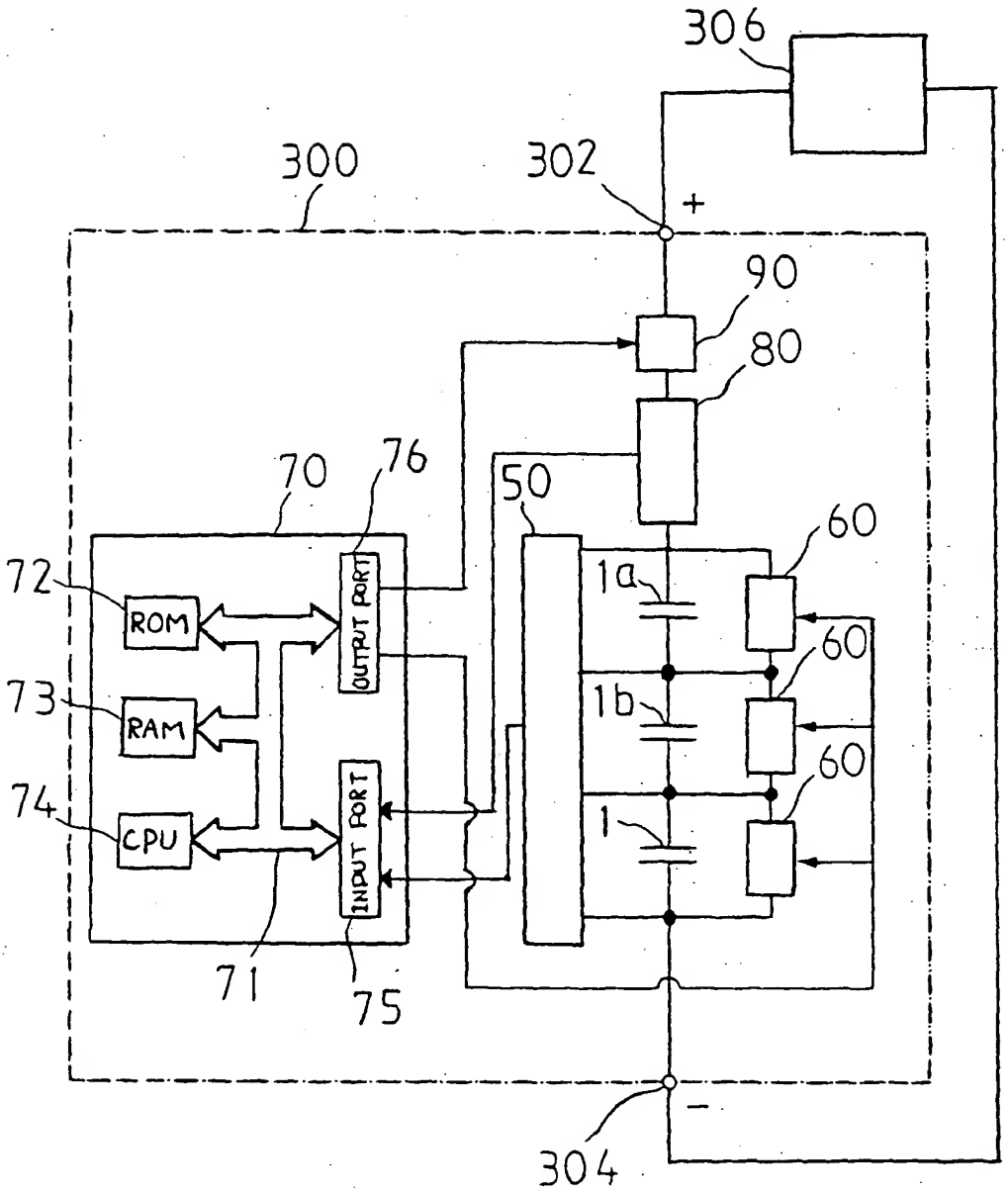

306
300
302
+
90
80
70
76
50
60
72
ROM
OUTPUT PORT
1a
60
73
RAM
1b
60
74
CPU
INPUT PORT
1
60
71
75
−
304

FIG. 8

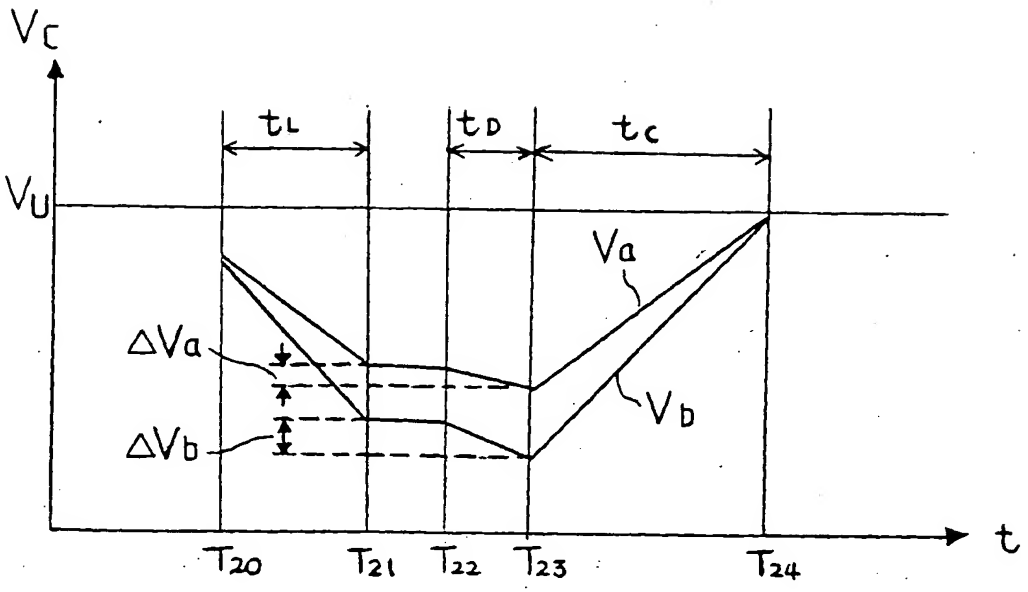


FIG. 9

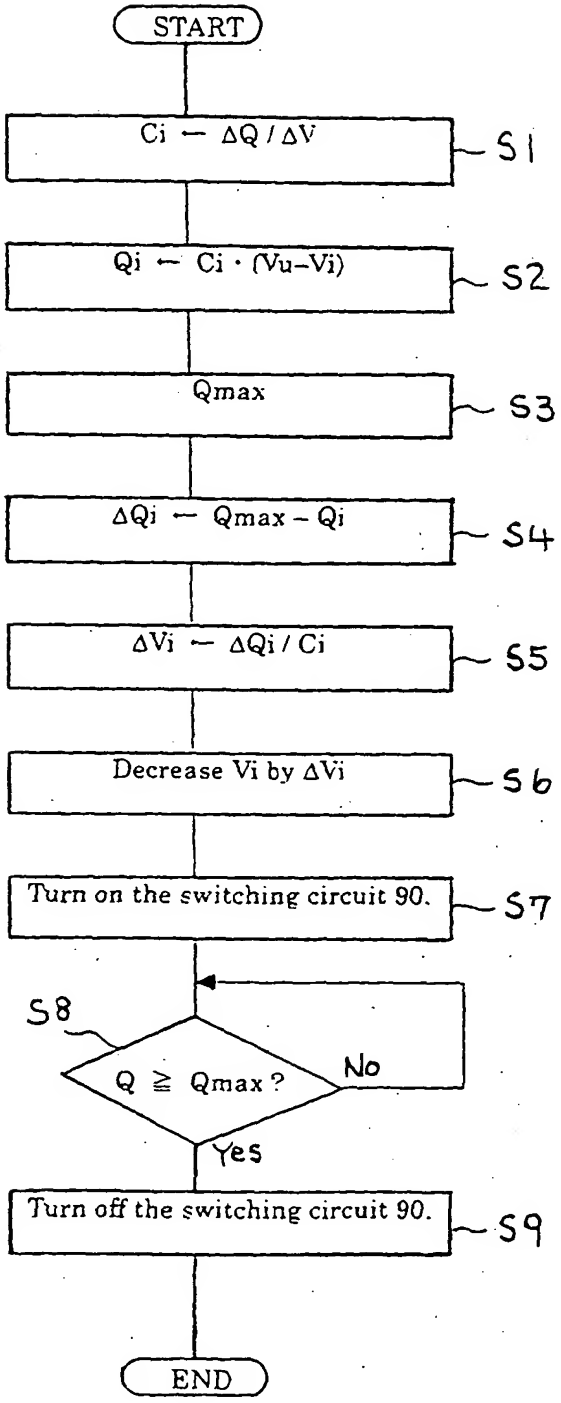

START
Ci ← ΔQ / ΔV
S1
Qi ← Ci · (Vu–Vi)
S2
Qmax
S3
ΔQi ← Qmax – Qi
S4
ΔVi ← ΔQi / Ci
S5
Decrease Vi by ΔVi
S6
Turn on the switching circuit 90.
S7
S8
Q ≧ Qmax ?
No
Yes
Turn off the switching circuit 90.
S9
END

FIG. 10

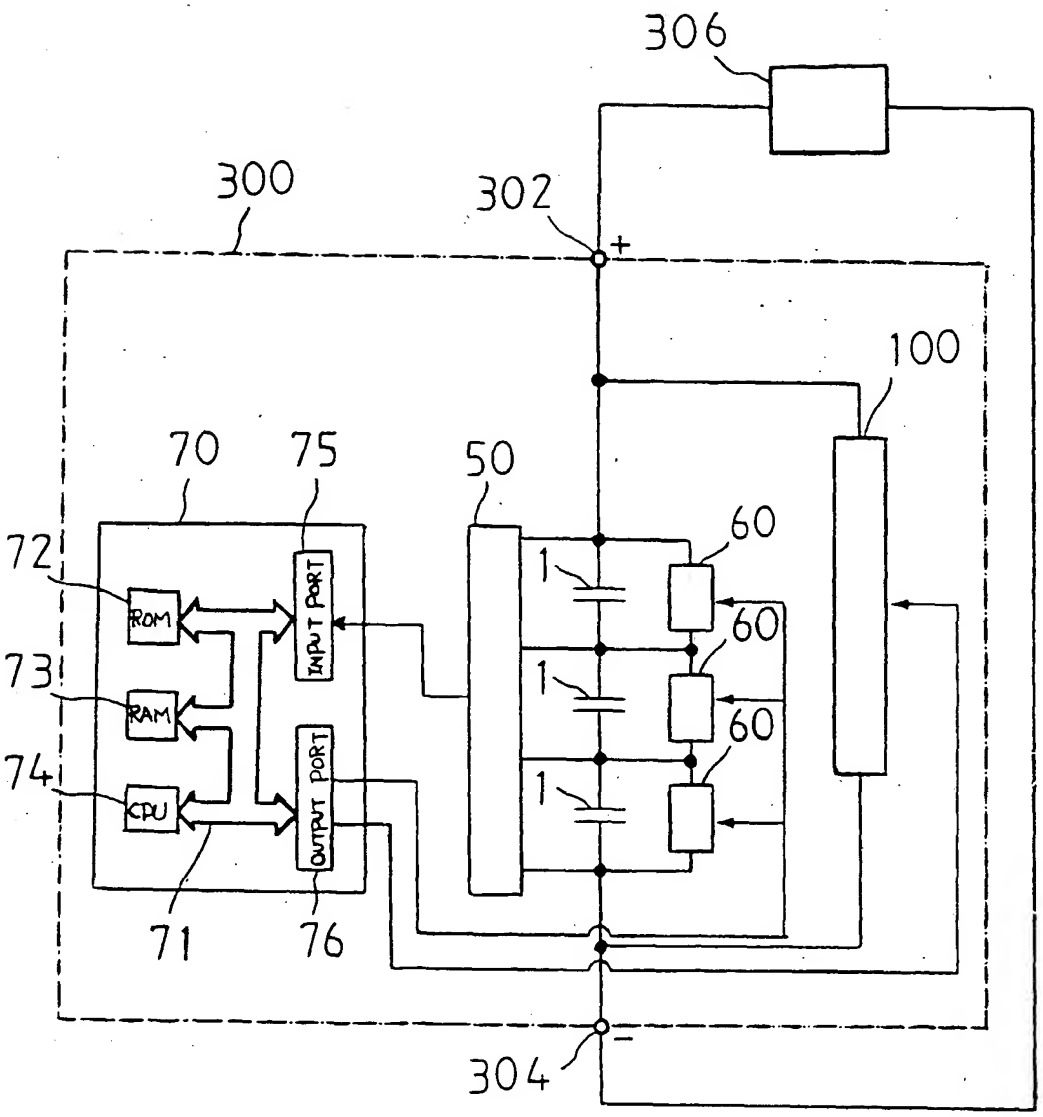

306
300
302
+
100
70
75
50
60
72
ROM
INPUT PORT
1
60
73
RAM
1
60
74
CPU
OUTPUT PORT
1
71
76
304
−

FIG. 11

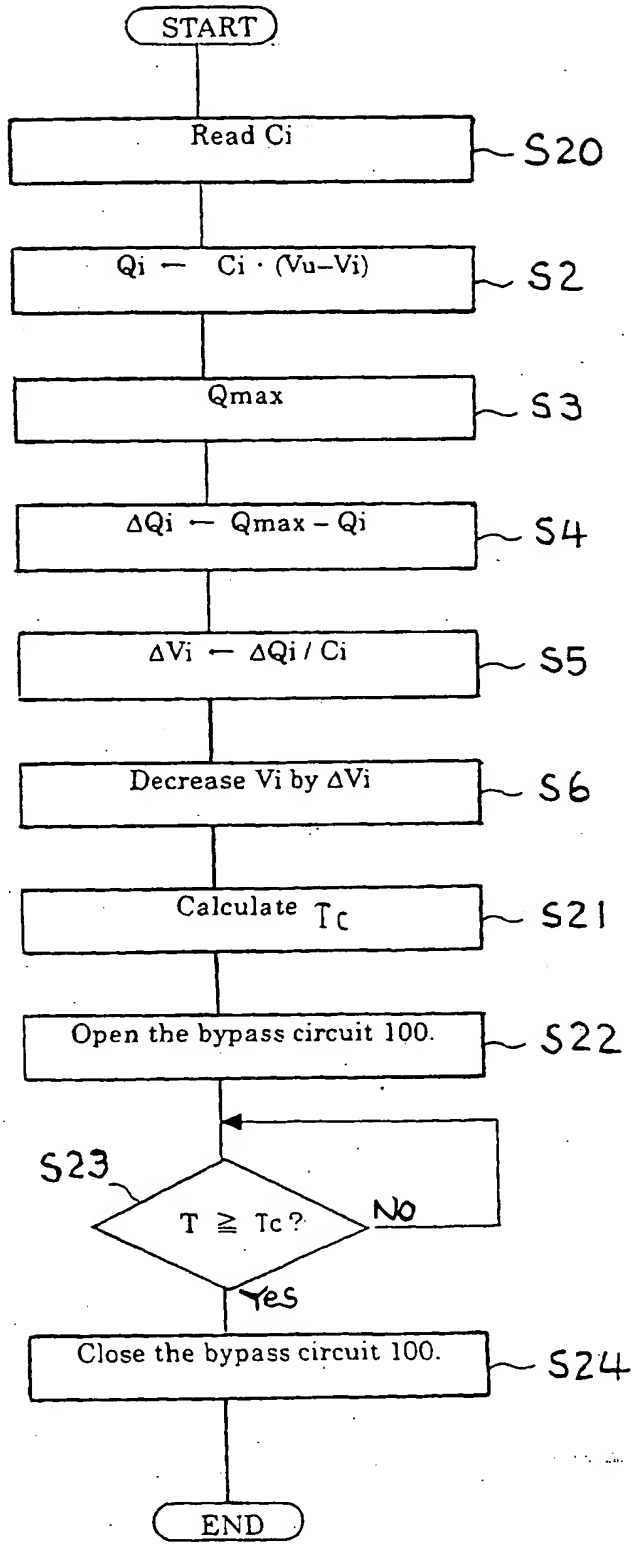

START
Read Ci
S20
Qi ← Ci · (Vu−Vi)
S2
Qmax
S3
ΔQi ← Qmax − Qi
S4
ΔVi ← ΔQi / Ci
S5
Decrease Vi by ΔVi
S6
Calculate Tc
S21
Open the bypass circuit 100.
S22
S23
T ≧ Tc ?
No
Yes
Close the bypass circuit 100.
S24
END

FIG. 12

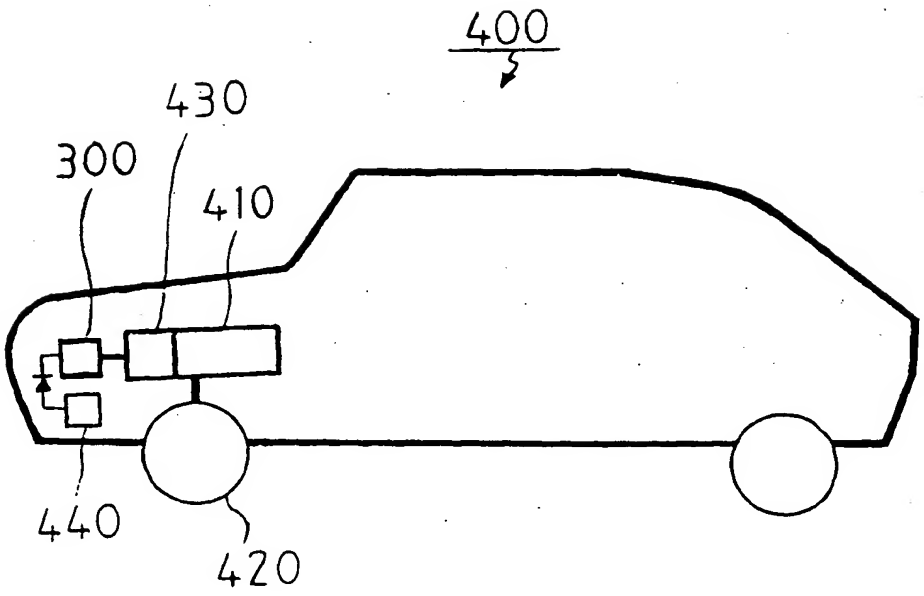


FIG. 13

(PRIOR ART)

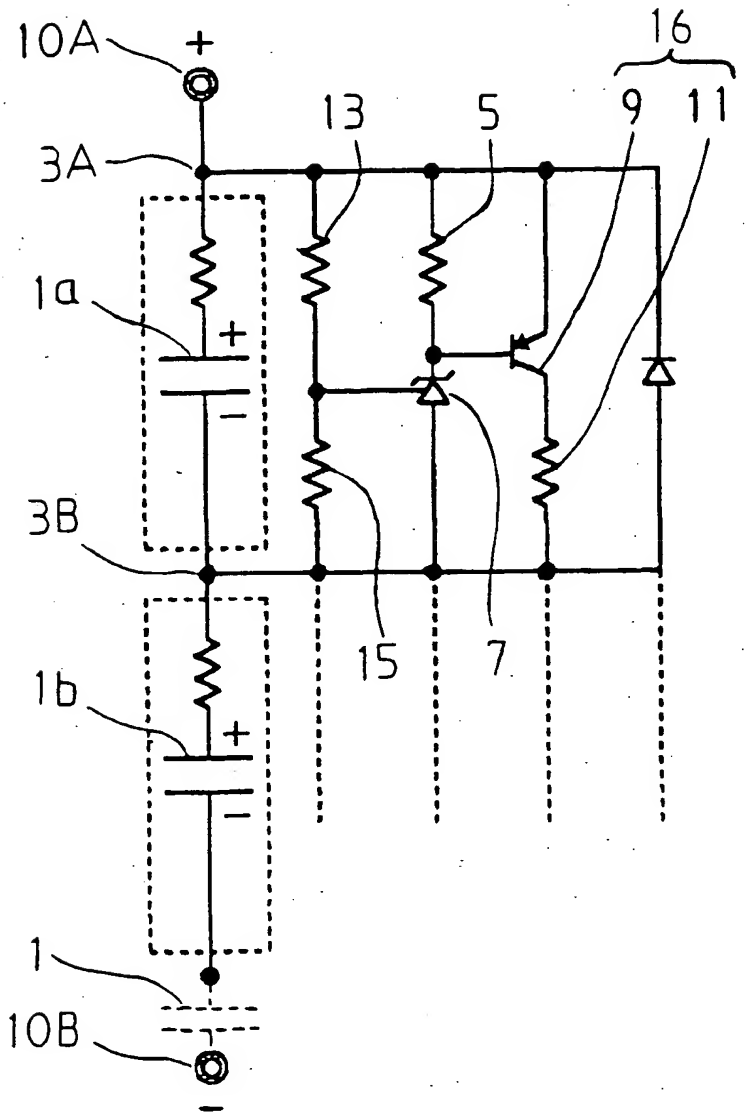


FIG. 14

(PRIOR ART)

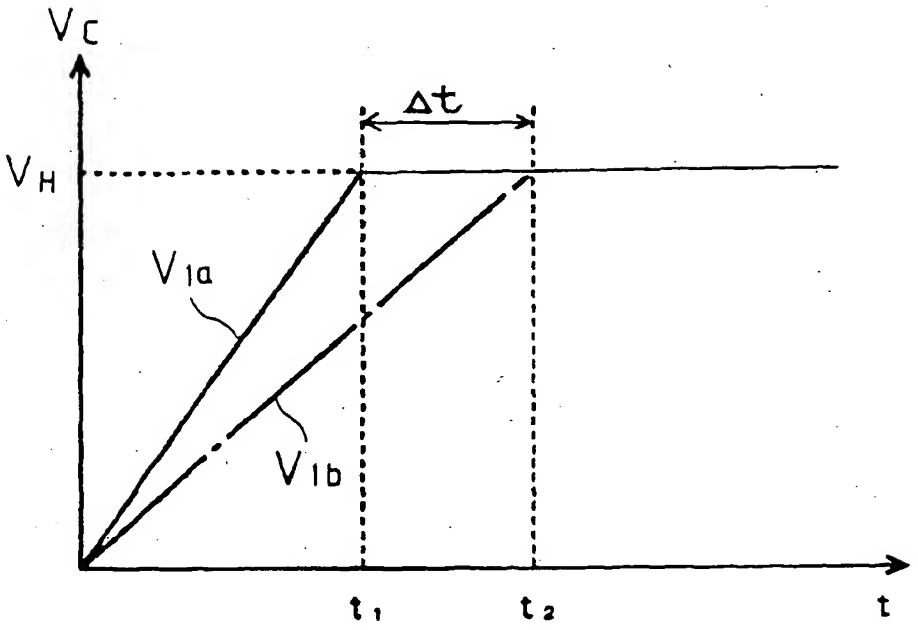
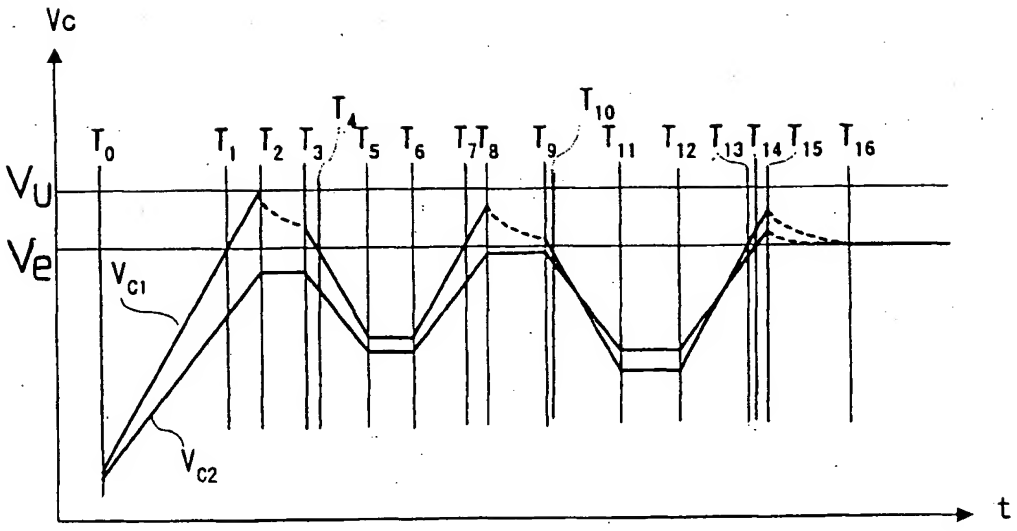


FIG. 15


Vc
T0
T1
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EUROPEAN SEARCH REPORT

Application Number
EP 00 10 4479

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 May 2000	Moyle, J

CATEGORY OF CITED DOCUMENTS

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